REMARKS

Claims 1-32 are pending in the present application, and stand rejected. Claim 28 has been amended. This application continues to include claims 1-32.

The Examiner rejected claims 1-5, 10, 11, 16-19, 28-32 under the judicially created doctrine of obviousness-type double patenting in view of claims in the copending application (09/859,782). In the copending application (09/859,782), claims 1, 9, 17, 23 and 27 are independent, and in the present 09/896,975 application, claims 1, 10, 19, 24 and 28 are independent. In the copending 09/859,782 application, claims 2-8 depend from claim 1, claims 10-16 depend from claim 9, claims 18-22 depend from claim 17, claims 24-26 depend from claim 23, and claims 28-31 depend from claim 27. In the present 09/896,975 application, claims 2-9 depend from claim 1; claims 11-18 depend from claim 10; claims 20-23 depend from claim 19; claims 25-27 depend from claim 24; and claims 29-32 depend from claim 28.

The Examiner asserts that, "The additional limitation of detecting and adjusting a communication rate is not a patentably distinct limitation, as it is well known in the art. The claimed support for differing communications standards also does not render the claimed invention unique, as a communications device could be readily adapted to any communications standard." Applicants, however, continue to believe that the subject claims in the present 09/896,975 application and the copending 09/859,782 application are patentably distinct.

In contrast to the claims of the copending 09/859,782 application, for example, independent claim 1 of the present 09/896,975 application requires the additional steps of "obtaining a communication link speed" and "calculating a sample count value of said counter using said communication link speed". Neither claim 1 of present 09/896,975 application nor claim 1 of the copending 09/859,782 application recite a "detecting" or "adjusting" limitation, as

asserted by the Examiner. Accordingly, independent claim 1 of the copending 09/859,782 application and independent claim 1 of the present 09/896,975 application are patentably distinct.

In contrast to independent claim 9 of the copending 09/859,782 application, independent claim 10 of the present 09/896,975 application recites, "determining a communication link speed" and "defining a sample count value of said counter utilizing said communication link speed." Claim 9 of the copending 09/859,782 application recites defining a sample count value of said counter, and does not further define the sample count as utilizing the communications link speed, nor does claim 9 recite a step of determining the communication link speed. The Examiner contends that, "The additional limitation of detecting and adjusting is not a patentably distinct limitation, as it is well known in the art." Neither claim 10 of present 09/896,975 application nor claim 9 of the copending 09/859,782 application recite a "detecting" nor an "adjusting" limitation. Accordingly, independent claim 9 of the copending 09/859,782 application and independent claim 10 of the present 09/896,975 application are patentably distinct.

In contrast to independent claim 17 of the copending 09/859,782 application, independent claim 19 of the present 09/896,975 application recites, "said speed input being adapted to receive a variable representative of a communication link speed and said clock signal input being adapted for receiving a clock signal, wherein said synchronous pulse generator processes *said clock signal, said communication link speed and said difference signal to generate a synchronous pul*se used for extracting data from said difference signal". In addition, neither claim 19 of the present 09/896,975 application nor claim 17 of the copending 09/859,782 application recite a "detecting" or an "adjusting" limitation. Accordingly, independent claim 17 of the copending 09/859,782 application and independent claim 19 of the present 09/896,975 application are patentably distinct.

The Examiner recognizes claim 24 of the present 09/896,975 application and claim 23 of the copending 09/859,782 application as being patentably distinct.

In contrast to independent claim 27 of the copending 09/859,782 application, independent claim 28 of the present 09/896,975 application recites "detecting a data speed", and "defining a sampling count value based on said data speed". In contrast to independent claim 28 of the present 09/896,975 application, independent claim 27 of the copending 09/859,782 application additionally recites "providing a single clock signal" and "sampling said data using said single clock signal when said pulse is asserted." Accordingly, independent claim 27 of the copending 09/859,782 application and independent claim 28 of the present 09/896,975 application are patentably distinct.

Accordingly, in view of the above, it is respectfully requested that the obviousness-type double patenting rejection be withdrawn.

Claims 1-19 and 22-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan (US 6,359,946). Claims 20-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of IEEE-1394b, Draft 1.11.

The grounds for rejection of claims 6-9 and 22-25 are unclear. While the stated grounds for rejection are under 35 U.S.C. § 103(a) as being unpatentable over Ryan, in rejecting claims 6-9 and 22-25 reference also is made to IEEE-1394b. Clarification is respectfully requested so that Applicants may appropriately respond to the rejection of claims 6-9 and 22-25. For example, claims 20-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of IEEE-1394b, Draft 1.11, but claims 6-9 and 22-25 were not.

Applicants respectfully request reconsideration of the rejection of claims 1-32 in view of the following.

Claim 1 recites, in part, a method for effecting synchronous pulse generation for use in serial communications, wherein "if said current count value corresponds to said sample count value then performing a step of generating a synchronous pulse, and if said current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed, and if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated."

The Examiner acknowledges that "Ryan is silent with respect to a difference signal", but further states that Ryan does teach a method of receiving serial communications of which difference signals are one of a known technique for the transmission of serial data and therefore would be a design choice according to the system application.

The reliance on "design choice" is unfounded, since Applicant's claimed invention recites limitations which rely on the generation of the difference signal and the way the difference signal is treated during operation, as more fully set forth below. Also, no explanation is provided as to how a modification by Ryan by "design choice" would yield Applicants' invention, as recited in claim 1. Ryan neither discloses accommodating a difference signal, nor the processing of the difference signal.

With respect to the "difference signal" clauses in claim 1, claim 1 first recites "*generating a difference signal representing a signal level difference between at least two data stream*

signals". In comparison, Ryan discloses a single data signal 10 (see Ryan Fig. 5). Accordingly, Ryan fails to disclose, teach or suggest even the initial act of *generating a difference signal representing a signal level difference between at least two data stream signals*.

In addition, claim 1 further recites the condition of "if said current count value does not correspond to said sample count value then performing a step of *determining whether a signal level of said difference signal has changed*, and if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal *until* said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated." Ryan does not disclose, teach or suggest, *determining whether a signal level of said difference signal has changed* if the current count value does not correspond to the sample count value, nor does Ryan disclose, teach or suggest "if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal *until* said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated."

Accordingly, Ryan does not disclose, teach or suggest the subject matter of claim 1, and thus, claim 1 is believed to be in condition for allowance in its present form.

Claims 2-9 depend, directly or indirectly, from claim 1. Accordingly, claims 2-9 are believed to be in condition for allowance in view of their dependence from claim 1, for the reasons set forth above with respect to claim 1. In addition, claims 2-9 further and patentably define the present invention over the cited references.

For example, claim 2 recites, "The method of claim 1, wherein said synchronous pulse is used to signify a time for performing a step of sampling said difference signal to extract data from

said difference signal." By the Examiner's admission, Ryan is silent with respect to a "difference signal" and thus, cannot disclose, teach or suggest using said a synchronous pulse to signify a time for performing a step of sampling said difference signal *to extract data* from said difference signal. In any event, in rejecting claim 2, the Examiner relies on Ryan Fig. 1 and column 13, lines 22-25. However, Ryan column 13, lines 22-25 recites, "The serial-to-parallel converter of FIG. 7 operates as follows. As the flip-flops 96 of the first shift register are clocked, a serial data word provided by serial data in signal 110 is shifted into the first shift register bit by bit." Accordingly, the cited passage from Ryan does not relate to sampling of a difference signal, but rather, is directed to a serial to parallel conversion.

In addition, Ryan Fig. 1 does not show the use of a *synchronous pulse*, generated when the current count value correspond to the sample count value, as defined in claim 1, to signify a time for performing a step of sampling the difference signal. In contrast, Ryan Fig. 5 discloses a receiving device/circuitry 200 that receives the data signal 10 (not a difference signal), the clock signal SCLK, and the "edge-to-close" signal 30. However, Ryan discloses that the edge-to-close signal 30 "may be used to alert other function blocks of the receiving device that the most recent sample may be incorrect" and in turn "may be used to cause the data signal 10 to be resampled". (Ryan, column 8, lines 11-14). Thus, the edge-to-close signal 30 is not a synchronous pulse that specifies a time for performing the step of sampling the difference signal. In Ryan, the data signal is sampled using the sample clock signal SCLK (see Ryan, column 6, line 66-column 7, line 12), and the edge-to-close signal 30 is used to alert other function blocks of the receiving device that the most recent sample may be incorrect. Accordingly, Ryan does not disclose, teach or suggest the subject matter of claim 2.

Claim 3 recites, "The method of claim 1, further comprising a step of defining a maximum

count value of said counter, wherein if said current count value corresponds to said maximum count value then performing a step of resetting said counter." In rejecting claim 3, the Examiner relies on Ryan column 9, lines 33-41, however, the cited passage makes no mention of a condition for resetting a counter. Rather, the cited passage discloses that the counter runs down on its own accord.

Claim 4 recites, "The method of claim 1, wherein said step of determining whether said signal level of said difference signal has changed comprises the steps of: checking said signal level of said difference signal each cycle of said clock signal; storing said signal level of said difference signal at a first clock cycle as a temporary difference signal; checking said signal level of said difference signal at a second clock cycle; and comparing said signal level of said temporary difference signal with said signal level of said difference signal at said second clock cycle." In rejecting claim 4, the Examiner relies on Ryan Fig. 3. However, Ryan Fig. 3 references a data signal, and not a difference signal "representing a signal level difference between at least two data stream signals".

Claim 5 recites, "The method of claim 1, wherein said step of ignoring further changes in said signal level of said difference signal further comprises the steps of: resetting said counter; determining whether said current count value corresponds to said sample count value; and if said current count value does not correspond to said sample count value then performing a step of incrementing said counter each cycle of said clock signal until said current count value corresponds to said sample count value at which time a step of sampling said difference signal to extract data from said difference signal is performed." In rejecting claim 5, the Examiner relies on Ryan column 9, lines 33-41 and column 10, lines 26-29. However, the cited passages do not address "ignoring further changes in said signal level of said difference signal", but rather, are

directed to adjusting "the frequency of clock signal 78" to "approximately match that of the data signal 10." (Ryan, column 9, lines 38-41).

With respect to Applicants claims 6-9, the Examiner recognizes that Ryan is silent with respect to IEEE-1394b communications link speeds, but concludes that it would be obvious to one of ordinary skill in the art to adapt Ryan's serial communications receiver to support IEEE-1394b communications link speeds. Applicants respectfully disagree. Ryan provides no motivation to adapt its teachings to apply to IEEE-1394b communications. Claims 6-9 are believed to be in condition for allowance in view of their dependence from claim 1.

Independent claim 10 is believed to be allowable for substantially the same reasons set forth above with respect to claim 1.

Claims 11-18 depend, directly or indirectly, from claim 10. Accordingly, claims 11-18 are believed to be in condition for allowance in view of their dependence from claim 10.

In addition, claims 11-18 further and patentably define the present invention over the cited references. For example, claim 11 is believed to be in condition for allowance for substantially the same reasons set forth above with respect to claim 2. Claims 12-15 are believed to be in condition for allowance for substantially the same reasons set forth above with respect to claims 6-9, respectively. Claims 16-18 are believed to be in condition for allowance for substantially the same reasons set forth above with respect to claims 3-5, respectively.

Claim 19 recites, in part, "a receiver having a first input, a second input and a first output, said first input being adapted for receiving a first data signal stream and said second input being adapted for receiving a second data signal stream, wherein said receiver processes said first data signal stream and said second data signal stream to generate a difference signal representing a difference between said first data signal stream and said second data signal stream". (Emphasis

added). As acknowledged by the Examiner, Ryan is silent with respect to a "difference signal, and the receiver of Ryan Fig. 5 does not include the "said first input being adapted for receiving a first data signal stream and said second input being adapted for receiving a second data signal stream" from which in turn the difference signal is generated.

In addition, claim 19, recites in part "a synchronous pulse generator having a first difference signal input, a clock signal input, a speed input and a synchronous pulse output, said difference signal input being coupled to said first output for receiving said difference signal, said speed input being adapted to receive a variable representative of a communication link speed and said clock signal input being adapted for receiving a clock signal, wherein said synchronous pulse generator processes *said clock signal, said communication link speed and said difference signal* to generate a synchronous pulse used for extracting data from said difference signal." (Emphasis added).

As set forth in Ryan, column 6, line 66-column 7, line 9, "Fig. 1 illustrates a timing diagram showing an asynchronous data signal 10 and a clock signal 16 *for sampling the asynchronous data signal 10.* Note that two alternative versions of clock signal 16 are illustrated in Fig. 1. One version shows a clock signal having a symmetrical duty cycle whereas the other version shows a clock signal with an asymmetrical duty cycle. These two versions of the clock signal are illustrated to show that the duty cycle of the sampling clock is not important. *Any* clock *signal providing a periodic edge* for sampling may be employed." In contrast, in claim 19, the synchronous pulse generator processes the *clock signal,* the *communication link speed and* the *difference signal* to generate a synchronous pulse used for extracting data from said difference signal.

Further, in rejecting claim 19, the Examiner relies on Ryan column 9, lines 30-33, as disclosing "said speed input being adapted to receive a variable representative of a communication link speed". Applicants find no support in Ryan to draw such a conclusion. The cited passage recites, "Bit-rate counter 60 may be programmed with a bit-rate value 72 that serves as a divide-by value to produce clock signal 78 at a frequency of the high speed clock divided by bit-rate value 72." (Emphasis added). In contrast, in claim 19 the speed input is adapted to receive a variable representative of a communication link speed, and not a "divide-by value" for a high speed clock as disclosed in the cited passage from Ryan.

Accordingly, Ryan does not disclose, teach or suggest the subject matter of claim 19, and thus, claim 19 is believed to be in condition for allowance in its present form.

Claims 22 and 23 depend, directly or indirectly, from claim 19. Accordingly, claims 22 and 23 are believed to be patentable in view of their dependence from claim 19.

Independent claim 24 recites, among other things, "a serial/parallel translator having a second clock input, a second difference signal input, a synchronous pulse input and an encoded data output, said second clock input being coupled to said first clock input for receiving said clock signal, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse, wherein said serial/parallel translator processes said clock signal, said difference signal and said synchronous pulse *to generate encoded data* for output on said encoded data output."

The Examiner asserts that Ryan teaches a serial interface engine, relying of Ryan Figs. 5 and 7, element 200, data signal 10 and clock signal SCLK, and column 13, lines 23-39. The language of column 13, lines 23-39, however, does not appear in claim 24, which recites

that "said serial/parallel translator processes said clock signal, said difference signal and said synchronous pulse *to generate encoded data* for output on said encoded data output." In contrast, out signal 112 of Ryan merely transfers the generated parallel data from the flip-flops in parallel at a particular time, and does not disclose using out signal 112, or elements 110, 96, 90, to generate encoded data.

In addition, claim 24 recites that the same "clock signal" is received at the first clock input of the synchronous pulse generator and at the second clock input of the serial/parallel translator. In contrast, Ryan Fig. 5 only discloses the input of generated clock signal SCLK to the receiving device/circuitry 200.

Accordingly, claim 24 is believed to be in condition for allowance in its present form.

Claims 25-27 depend, directly or indirectly, from claim 24. Accordingly, claims 25-27 are believed to be in condition for allowance in view of their dependence from claim 24.

Claim 28, as amended, recites, in part, and "sampling said data using said single clock signal when said pulse is asserted." In rejecting independent claim 28, the Examiner concedes that Ryan is silent with sampling data when a pulse is asserted. Ryan in fact discloses at column 6, line 66-column 7, line 9, "Fig. 1 illustrates a timing diagram showing an asynchronous data signal 10 and a clock signal 16 *for sampling the asynchronous data signal 10*. Note that two alternative versions of clock signal 16 are illustrated in Fig. 1. One version shows a clock signal having a symmetrical duty cycle whereas the other version shows a clock signal with an asymmetrical duty cycle. These two versions of the clock signal are illustrated to show that the duty cycle of the sampling clock is not important. *Any* clock *signal providing a periodic edge* for sampling may be employed." In contrast, in claim 28, the data is sampled "using said single clock signal when said pulse is asserted." (Emphasis added). Thus, the sampling in claim 28 does not

occur merely with respect to a clock signal, but rather, the sampling of the data occurs based on "detecting a change in said data; incrementing said count value if no change in said data is detected; generating a pulse when said counter reaches said sampling count value; and sampling said data using said single clock signal when said pulse is asserted." Accordingly, the sampling of data when the pulse is asserted is not a mere matter of "design choice", but rather, is a result of a novel sequence of events that define when the data sampling is to occur.

Accordingly, claim 28 is believed to be in condition for allowance in its present form.

Claims 29-32 are believed to be allowable due to their dependence from claim 28.

Accordingly, in view of the above, it is respectfully requested that the Examiner withdraw the rejection of claims 1-19 and 22-32 under 35 U.S.C. § 103(a) as being unpatentable over Ryan.

Claims 20-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of IEEE-1394b, Draft 1.11.

Claim 20 recites, in part "a serial/parallel translator having a second difference signal input, a synchronous pulse input and an encoded data output, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse, and said serial/parallel translator processing said difference signal and said synchronous pulse *to generate encoded data*, said *encoded data being output on said encoded data output*". (Emphasis Added).

With respect to claim 20, Ryan does not disclose, teach or suggest using a second difference signal input receiving the difference signal, nor does Ryan disclose, teach or suggest generating encoded data based on the processing of the difference signal and the

synchronous pulse. As such, the combination of Ryan with IEEE-1394b, as asserted by the Examiner, would not yield Applicants' invention, as recited in claim 20.

The Examiner asserts that Ryan Figs. 5 and 7, element 200, data signal 10, clock signal SCLK and column 13, lines 23-39, discloses a synchronous pulse input for receiving the synchronous pulse. In this regard, Ryan states at column 13, lines 25-30 that, "When the serial data has been shifted in to the desired parallel data word length, control logic 104 asserts out signal 112 which causes parallel data word out logic 90 to accept a bit of the parallel data word from the output of each of the flip-flops 96 in parallel." However, in claim 20, for example, the serial/parallel translator processes the synchronous pulse, along with at least one other signal, "to generate encoded data *for output* on said encoded output." In contrast, out signal 112 of Ryan merely transfers the generated parallel data from the flip-flops in parallel at a particular time, and does not disclose using out signal 112 to generate encoded data. Accordingly, the combination of Ryan and IEEE-1394b would not yield Applicants' invention, as recited in claim 20.

For reasons set forth above, claim 20 is believed patentable in its own right.

In addition, claims 20 and 21 are believed patentable due to their dependence from claim 19, since IEEE 1394b does not overcome the deficiencies of Ryan with respect to claim 19.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of IEEE-1394b, Draft 1.11.

For the foregoing reasons, Applicants submit that the present application is in condition for allowance in its present form, and it is respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (317) 894-0801.

Respectfully submitted,

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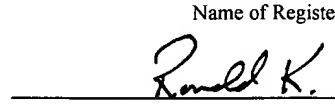

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